WHAT IS CLAIMED IS

1. A method for manufacturing a non-volatile memory array having vertical transistors, comprising the steps of:

providing a semiconductor substrate having trenches;

implanting dopants into the semiconductor substrate to form first doping regions and second doping regions at different heights, wherein the first doping regions are underneath the bottom of the trenches, and the second doping regions are beside the top of the trenches;

forming a gate dielectric layer on the semiconductor substrate, wherein the gate dielectric layer comprises at least one nitride film; and

forming conducting plugs in the trenches.

2. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 1, wherein the first and second doping regions are of a first conductive type selecting from one of N type and P type.

3. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 1, wherein the gate dielectric layer is an oxide/nitride/oxide layer.

4. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 1, further comprising an oxidization step to form edge insulation layers on sidewalls of the trenches and insulation blocks on the first and second doping regions, wherein the insulation blocks are thicker than the edge insulation layers.

5. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 1, further comprising a thermal process after the implanting step to diffuse the dopants within the first doping regions for connecting the first doping regions.

6. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 1, wherein the conducting plugs are polysilicon plugs.

7. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 6, wherein the polysilicon plugs are formed by the steps of:

depositing a polysilicon layer to fill up the trenches; and

planarizing the polysilicon layer.

8. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 1, further comprising the steps after the conducting plugs are formed:

depositing a polycide layer;

forming polycide lines and holes by masking and etching the polycide layer and the conducting plugs, wherein the polycide lines are substantially perpendicular to the first and second doping regions, and the holes divide the conducting plugs into pieces; and

forming an oxide layer in the holes and between polycide lines for isolation.

9. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 8, further comprising the step of forming an etch stop layer on the polycide layer after depositing the polycide layer.

10. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 8, further comprising the step of planarizing the oxide layer after the oxide layer is formed.

11. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 2, further comprising the step of

implanting dopants of a second conductive type to form third doping regions beside the trenches for channel profile adjustment of the vertical transistors.

12. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 11, further comprising the step of implanting dopants of the first conductive type to form fourth doping regions beside the trenches, wherein the third doping regions are located higher than the fourth doping regions.

13. A method for manufacturing a non-volatile memory array having vertical transistors, comprising the steps of:

providing a semiconductor substrate having trenches;

implanting dopants of a first conductive type into the semiconductor substrate to form first doping regions underneath the bottom of the trenches;

forming a gate dielectric layer on the semiconductor substrate, wherein the gate dielectric layer comprises at least one nitride film; and

forming conducting plugs in the trenches; and

implanting dopants of the first conductive type into the semiconductor substrate to form second doping regions beside the top of the trenches.

14. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 13, further comprising a thermal process to diffuse the dopants within the first doping regions for connecting the first doping regions.

15. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 13, wherein the conducting plugs are polysilicon plugs.

16. A method for manufacturing a non-volatile memory array having vertical transistors, comprising the steps of:

providing a semiconductor substrate having trenches;

filling the trenches with blocking plugs;

implanting dopants of a first conductive type into the semiconductor substrate to form second doping regions beside the top of the trenches;

removing the blocking plugs;

implanting dopants of the first conductive type into the semiconductor substrate to form first doping regions underneath the bottom of the trenches;

forming a gate dielectric layer on the semiconductor substrate, wherein the gate dielectric layer comprises at least one nitride film; and

forming conducting plugs in the trenches.

17. The method for manufacturing a non-volatile memory array having vertical transistors of Claim 16, wherein the blocking plugs are composed of photoresist.

18. A non-volatile memory array having vertical transistors, wherein at least one of the vertical transistors is formed in a trench of a semiconductor substrate and comprises:

a first doping region of a first conductive type being underneath the bottom of the trench;

a second doping region of the first conductive type being beside the top of the trench;

a gate dielectric layer formed on the first doping region, the second doping region and the sidewall of the trench, wherein the gate dielectric layer comprises at least one nitride film; and

a conducting plug formed in the trench.

19. The non-volatile memory array having vertical transistors of Claim 18, wherein the semiconductor substrate is constituted of a silicon substrate and a mask layer.

20. The non-volatile memory array having vertical transistors of Claim 19, wherein the mask layer is selected from the group of silicon nitride, silicon oxide, silicon oxynitride and multi-layer thereof.

21. The non-volatile memory array having vertical transistors of Claim 19, wherein the mask layer is of a thickness between 100 to 2000 angstroms.

22. The non-volatile memory array having vertical transistors of Claim 18, wherein the first and second doping regions functions as bit lines for the non-volatile memory array.

23. The non-volatile memory array having vertical transistors of Claim 18, wherein the gate dielectric layer is an oxide/nitride/oxide layer.

24. The non-volatile memory array having vertical transistors of Claim 23, wherein the oxide/nitride/oxide layer is of a thickness between 60-500 angstroms.

25. The non-volatile memory array having vertical transistors of Claim 18, wherein the conducting plugs are polysilicon plugs.

26. The non-volatile memory array having vertical transistors of Claim 18, wherein the at least one of the vertical transistors further comprises insulation blocks formed on the surfaces of the first and second doping regions.

27. The non-volatile memory array having vertical transistors of Claim 26, wherein the at least one of the vertical transistors further comprises edge insulation layers formed on sidewalls of the trenches, and the insulation blocks are thicker than the edge insulation layers.

28. The non-volatile memory array having vertical transistors of Claim 18, wherein the at least one of the vertical transistors further comprises a third region of a second conductive type beside the trench.

29. The non-volatile memory array having vertical transistors of Claim 28, wherein the at least one of the vertical transistors further comprises a fourth doping region of the first conductive type beside the trench, and the third doping region is located higher than the fourth doping region.

30. The non-volatile memory array having vertical transistors of Claim 18, wherein the first doping regions of the vertical transistors are connected as one of a common source and a common drain.

31. A non-volatile memory array having vertical transistors, wherein at least one of the vertical transistor is formed in a trench of a semiconductor substrate and comprises:

a first doping region of a first conductive type being underneath the bottom of the trench;

a second doping region of the first conductive type being beside the top of the trench;

a gate dielectric layer formed on the first doping region, the second doping region and the sidewall of the trench, wherein the gate dielectric layer comprises silicon nanocrystal particles; and

a conducting plug formed in the trench.

32. The non-volatile memory array having vertical transistors of Claim 31, wherein the density of the silicon nanocrystal particles is in the range of $5x10^{11}$ to $5x10^{12}cm^{-2}$.